High Frequency AGC Has Digital Control

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Introduction

Many systems (especially communications) require an AGC which will function at 50MHz. Self-calibrating systems such as automatic test equipment also need the high frequency response, but they add a requirement that the AGC output voltage be set by a digital signal. During the calibration cycle this test equipment will calculate the AGC output voltage needed to achieve the accuracy requirements, and they will increment the AGC output voltage until the system is within specifications. The AGC circuit described in Figure 1 uses a DAC to accomplish the digital control, and because the DAC is the reference input for the AGC circuit, it ultimately sets the AGC output voltage. The HI5731 was chosen for the DAC because it is inexpensive, it functions with 5V supplies, the output interfaces well with the AGC circuit, and it can be updated at a 100MHz rate. The heart of the AGC circuit is a variable gain amplifier made from a three transistor, long-tailed pair configuration, Q_1, Q_2, and Q_3. When the base voltage of Q_3 is varied the emitter current of the long-tailed pair changes, forcing a gain change according to the following equation, where K is a function of the emitter current and V_{B3} is the base voltage of Q_3:

$$G = KV_{IN}|V_{B3}| \quad \text{(EQ. 1)}$$

The gain-control and bias-stability parameters of the circuit depend on the transistor matching, so the circuit uses a HFA3102-matched, long tailed array for Q_1 through Q_3. The usable range of V_{B3} is -0.04 to -4.1V, which corresponds to a gain range of 0.8 to 17.6dB, respectively (V_{IN} = 100mV). This gain span is a total of 16.8dB. The gain is proportional to R_4. Increasing R_4 increases the gain, but the gain span stays constant at approximately 16.8dB while the frequency response decreases.

The gain span limits the AGC circuit's ability to compensate for input voltage changes greater than the gain span, 16.8dB. If the input voltage change will exceed the gain span it can be almost doubled by putting two long-tailed pair in series; this is aided by the HFA3102 because it contains two long-tailed pairs. AC connect the collectors of the first stage differently to the bases of the second stage. Connecting the bases of the current source transistors in parallel enables the AGC circuit to maintain the same control function, while the gains of the two long-tailed pairs are multiplied thus, essentially doubling the gain span.

The input signal is amplified by the long-tailed pair to make the gained up output signal, which in turn is half-wave rectified by the HFA1103 to produce a quasi DC control voltage. The HFA1103 is a high speed op amp that has the lower half of the output stage disconnected, so because the output can't go below ground it make a fine half wave rectifier or sync stripper. R_9, through R_{12} set the gain to two, and add a few mV of bias to ensure that the output is always positive. This DC voltage is compared with the DAC output voltage in the input stage of the CA5160 integrator. Because the integrator has a large DC gain it's output voltage will swing to any point within the supplies in an attempt to lock the loop. The DAC output sinks current from ground. R_5 and R_{16} form a voltage divider with DC offset, and this DC voltage, which is the reference input, V_R, for the AGC circuit, is compared with the output of U_1 in the integrator, U_2.

The signal path has excellent frequency response because the HFA3102 is the only component in the signal path. The control path through U_1 does not have quite as good a frequency response, so R_4 or the input signal must be increased to provide control past 50MHz. The DAC transfers the digital input to an internal register on the rising edge of the clock pulses. The circuit uses the non-inverting DAC output to yield a positive-increasing transfer function, but you can obtain the inverse-transfer function by using the inverting DAC output (Table 1).

TABLE 1. AGC PERFORMANCE SUMMARY

PARAMETER	MINIMUM	MAXIMUM
Gain (dB)	0.8	17.6
V_{B3} (V)	-0.04	-4.1
V_R (V)	-0.045	-0.275
Digital Input/Non-Inverting Output	1111 1111 1111	0000 0000 0000 0000
Digital Input/Inverting Output	0000 0000 0000 0000	1111 1111 1111 1111

Fast DAC updates will not affect the output signal with the selected value of C_1 = 1µF because the integrator filters out the change. When the DAC updates, the output voltage will slowly change to the new value. If the circuit is only used for system calibration where slow DAC updates are the rule, you can use a slower DAC. However, you may have to redesign the interface circuit (U_2 and associated components) if the DAC output current swing changes. If the value of C_1 is decreased the amplitude of the output signal will tend to follow the DAC updates, thus, if the DAC updates are done in a sinusoidal manner the output signal will be amplitude modulated by the DAC update frequency.

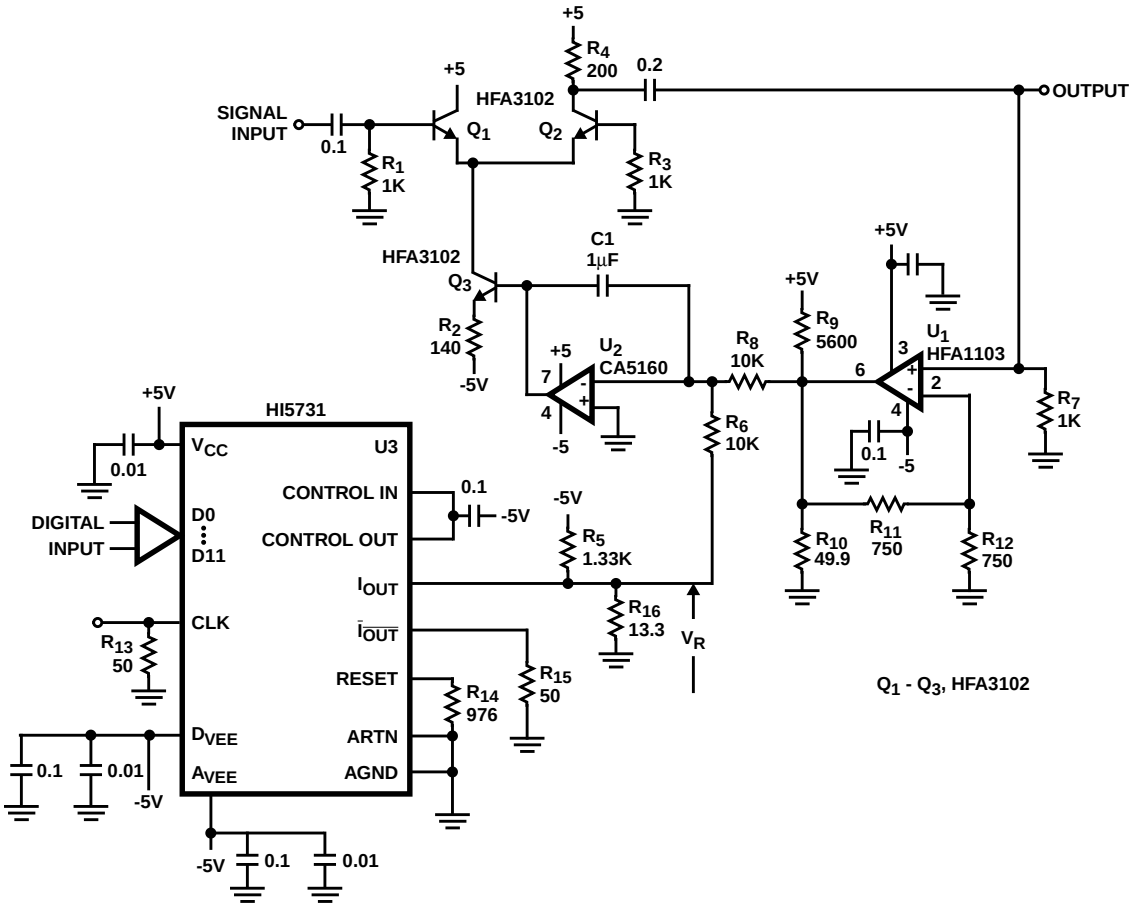

FIGURE 1. HIGH FREQUENCY AGC HAS DIGITAL CONTROL